Design and Development of Digital control based Asymmetric Multilevel Inverter for Renewable Energy Systems

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Abstract: **Multilevel inverter is an effective topology for increasing power demand and reducing harmonics of AC waveforms. This paper presents an efficient seven-level asymmetric cascaded multilevel inverter suited for renewable energy applications. A digital control method employing flip-flops has been proposed which reduces Total Harmonic Distortion (THD) and switching losses compared to the conventional PWM technique. Various performance parameters namely THD, switching loss, first-order distortion factor (DF1) and second-order distortion factor (DF2) is analyzed and a simulation model of the proposed digital control is developed in MATLAB/SIMULINK. Hardware prototype will be built to validate the results.**

Index terms: **Asymmetric multilevel inverter, digital control, THD & DF.**

I. Introduction

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms[1,2]. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductor must withstand only reduced voltages. By synthesizing the AC output terminal voltage from several levels of DC voltages, staircase output waveform can be produced. This allows for higher output voltage and simultaneously lowers the voltage stress in the switch. Furthermore, as the number of voltage levels on the Dc side increases, the synthesized output adds more steps, producing an output which approaches the sinusoidal wave with minimum harmonic distortion. Several topologies for multilevel inverters have been proposed in the literature, the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. This paper presents multilevel inverter consisting of series connection of separate single full bridges on the ac output terminals. This topology is suitable for applications where separate DC voltage sources are available, such as photovoltaic (PV) generators, fuel cells and batteries[3]. A novel digital control technique has been proposed for the asymmetric cascaded multilevel inverter. To investigate the importance of the proposed digital scheme, various performance parameters are calculated and the simulation is performed using MATLAB. An experimental test circuit has been built to validate the simulation results.

II. Asymmetric cascaded multilevel inverter

Conventionally, each phase of a cascaded MLI requires 'm' dc sources to produce (2m+1) levels. For the asymmetric cascaded MLI, a scheme is proposed which allows the use of two unequal dc sources (such as battery or fuel cell). A seven-level hybrid cascaded MLI has two H-bridge for each phase. One H-bridge is connected to a dc source of value V_{dc} and another is connected to a dc source of value $0.5V_{dc}$, as shown in Fig.1. The output voltage of the first H-bridge (H_1) is denoted by V_1, and the output of the second H-bridge (H_2) is denoted by V_2 so that the cascaded output voltage of the MLI is $V(t) = V_1(t) + V_2(t)$. By opening and closing the switches of H_1 appropriately, the output voltage V_1 can be made equal to $-V_{dc}$, 0, or $+V_{dc}$ while the output voltage of H_2 can be equal to $-0.5V_{dc}$, 0, or $+0.5V_{dc}$. Therefore, the MLI produces the seven levels as 0, V_{dc}, $2V_{dc}$, $3V_{dc}$, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ which is shown in Fig.2.

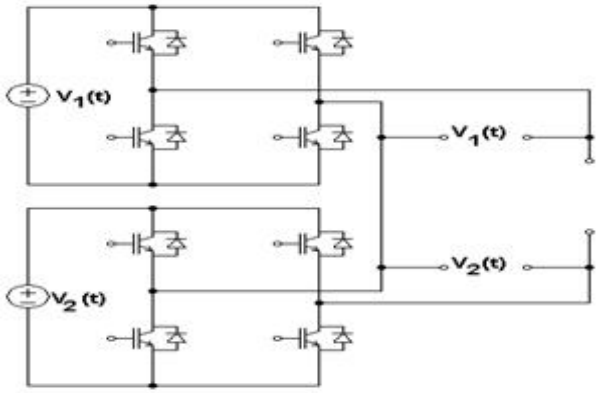

Fig.1 Circuit Diagram of Single-phase Asymmetric MLI

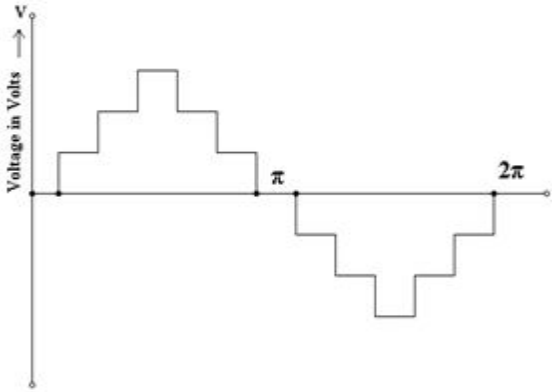

Fig.2 Seven-level output waveform

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III. Digital Modulation For Mli

Digital modulation for multilevel inverter has two stages, which is similar to that of the conventional, each inverter is operated to give three voltage levels (zero, positive DC voltage and negative DC voltage). This is achieved only by making a suitable firing sequence[4,5]. The inverters are fed with various DC input voltages are connected in series across the output to provide voltage at different levels. This mode of operation helps to achieve increased number of levels with use of three sources at different voltage level. The seven level waveform of cascaded inverter is shown in the Fig.2.Thus in the proposed model we are able to obtain the output levels of 2^{n+1}-1. All the inverters are operated at fundamental frequency. Here we use two inverters fed with voltage scaled in the power of two. So, this helps to achieve output level in the range of 2^n. This is possible with the help of binary counter which produces an output in the range of 2^n for counting n bits; this output is used to drive the inverter switches to get 2^n level in one half cycles. As a desirable characteristic for switching the power switches, the upper leg switches of all the inverters (T11 and T21) is in ON condition for a period of 10ms (i.e., for positive half cycle). Similarly for negative half cycle the lower leg switches (T13 and T23) is in ON state for 10-20ms. This consequently reduces the switching losses occurring at that particular switch. Also the diodes across the power switch helps in two ways by providing freewheeling path and closing the circuit. The voltage at the output is brought to the required level either by switching ON/OFF the switch in one of the inverter or any two or all the inverters. According to the Fig.2 of the proposed model the inverters are connected in series with no special requirements in design. A truth table given in Table.1 gives the sequence to trigger the switch in a particular inverter to change the output voltage level[6,7]. As combination with two stage voltage levels with a difference of 10V between each level can be obtained. So this helps to get a maximum level of 30V at the output.

Table I. Truth Table for Triggering the switches

Positive Half Cycle			Negative Half Cycle		
In 2	In 1	V_o	In 2	In 1	V_o
0	1	10	0	1	-10
1	0	20	1	0	-20
1	1	30	1	1	-30
1	1	30	1	1	-30
1	0	20	1	0	-20
0	1	10	0	1	-10

The power switches in the inverter are operated in a sequence resembling the truth table of a counter. Thus for implementing a multilevel inverter with the requirements of the above said firing sequence, it needs n+2 bit counters.Fig.3 shows the block diagram of firing unit. The counter is operated in the conventional manner so that it acts as an up counter. The logic circuit is a combinational circuit which makes the output two bits (Q1 and Q2) to run in forward for the first half of the positive cycle and in reverse for the second half of the positive cycle and similarly in the negative cycle.

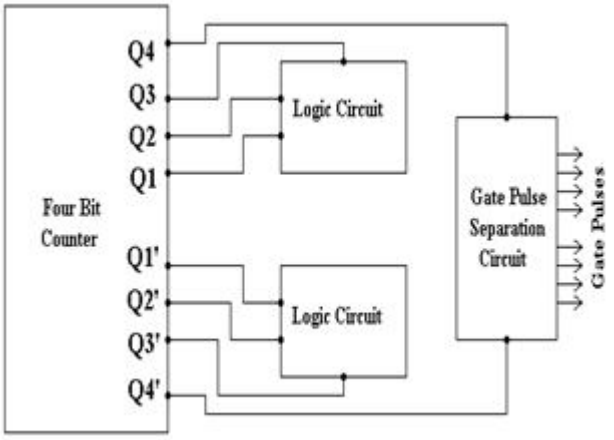

Fig.3 Block diagram of firing unit for digital modulation

This operation of modifying the two bits is done using the bits Q3 andQ3'. During the first half of the positive or negative cycle the count has to increment in such a way to increase the output voltage; this is controlled by the bit Q3'. Similarly the voltage has to descend in steps in the latter half of the positive or negative cycle; this is done by the bit Q3. The pulse separation circuit is also a combinational circuit which separates the pulses for positive and negative cycle. This operation is done with the help of bits Q4' and Q4 which is used as control bits in the circuit. In the proposed methodology of multilevel inverter, it is simulated using DC sources of 10V and 20V which are scaled in the multiples of two. The main methodology of proposed model resides basically on the counter. Since MATLAB does not support the counter operation directly, an asynchronous counter is constructed using J-K flip-flops. Then some logical operation is performed on the output of the counter to separate the pulses, which is to be given to the power switch. A logical conversion of Boolean to double is done with the help of a data conversion block. Since the MOSFET accepts the signals in the form of double for its gate it is necessary to convert the data type.

The firing circuit can be divided into three main parts as counter stage, logic circuits and the pulse separation circuit. The counter is operated in a normal manner as an up counter hence it counts the bits 0000 to 1111. The bits Q3 and Q4 at the output are used as control bits for the logic circuit and pulses separating circuit respectively[9,10]. Fig.4 shows the MATLAB simulation for the proposed digital control circuit. The logic circuit consists of AND and OR gates which are fed with bits Q1, Q2 and their complements. The control bit is the Q3 of the counter. This circuit makes the output to run forward and to run backward in the same manner, the output of this circuit is from 00 to 11 and from 11 to 00. The pulse separation circuit consists of AND, OR and EXOR gates which

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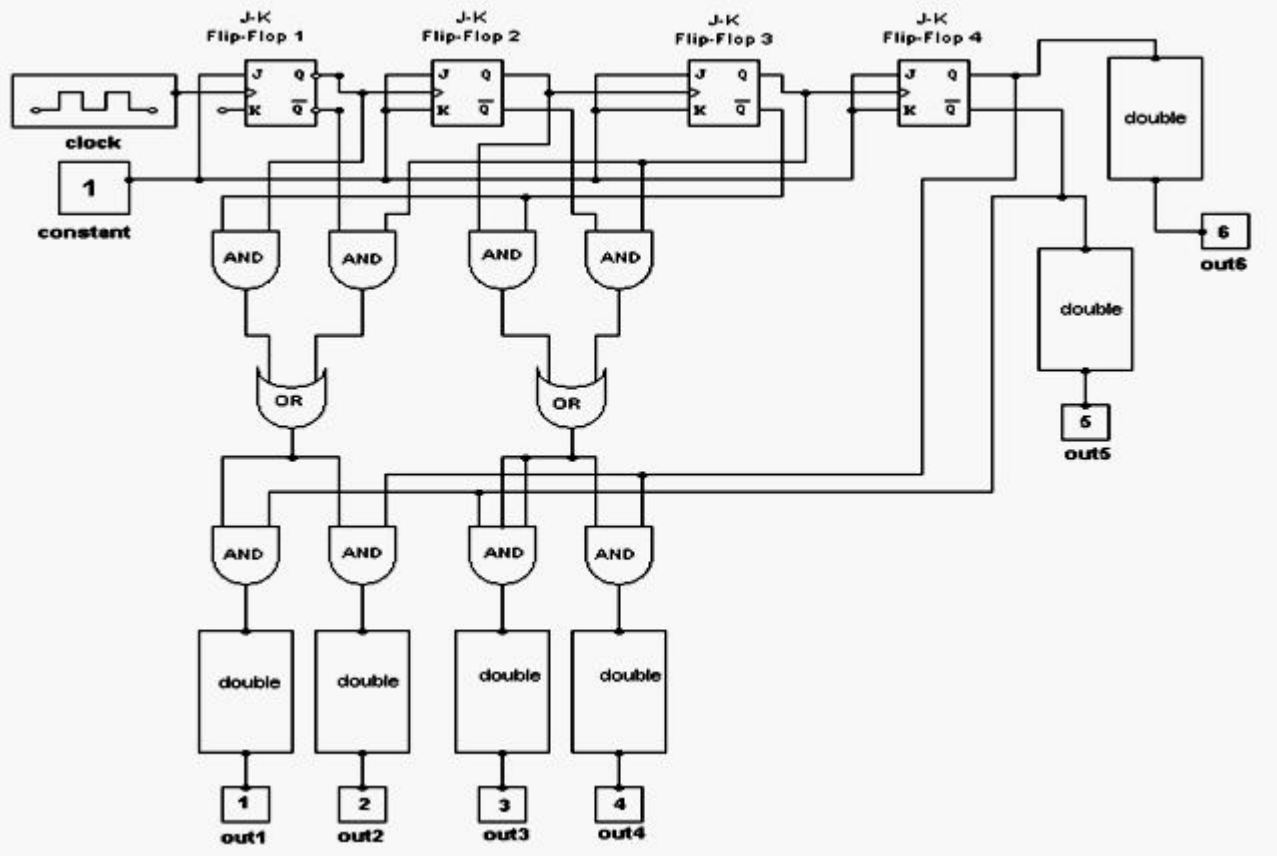

Fig.4. MATLAB implementation for digital modulation method

is fed with the output of the logic circuit. The bit Q4 acts as the control bit for separating the pulses in the positive and negative cycle. Hence the bits Q3 and Q3' helps to make the output to run in forward and backward direction simultaneously. The bits Q4 and Q4' helps to control the pulses to the positive and negative cycle. Hence the output frequency of the bit Q4 will be same as the output power frequency. Each half of the positive or negative cycle in the output of inverters resembles the output of the counter.

IV. Simulation results

The simulation for the proposed model of multilevel inverter was carried out with R load. As an inference from the simulation, the number of stage or the level increases the harmonics in the output is reduced. But the connected filters must be capable of suppressing the frequency components other than the power frequency. Even though each inverter is operated in the fundamental frequency, the switches are switched more than thrice of the power frequency in the base inverter. So in such conditions the connected filter must be able to reduce the harmonics produced due to switching.

The seven-level output of asymmetric cascaded MLI using Digital Modulation is shown in Fig.7.

The performance parameter such as Total Harmonic Distortion (THD), First-order Distortion Factor (DF_1), Second-order Distortion Factor (DF_2)[11] and switching losses has been evaluated using MATLAB. It was found that the proposed strategy has reduced THD compared to the conventional one as shown in Table: 2.

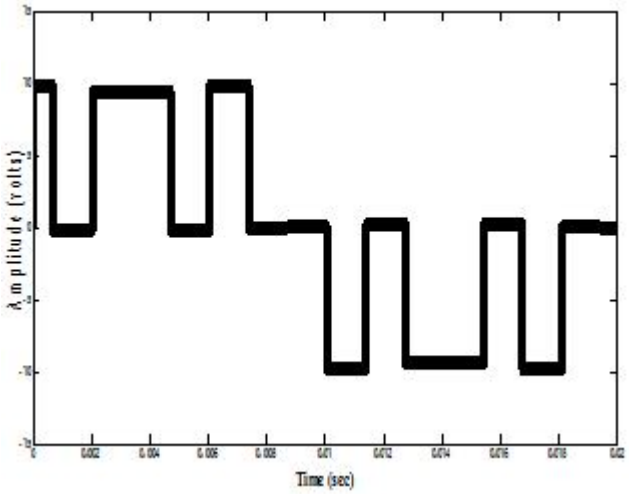

Fig.5 Output of bridge H_1

V. Experimental Results

To implement the hybrid cascaded seven-level inverter in an effective way, Transformers, bridge rectifier and voltage regulators are used to form 12V DC supply for opto-couplers. Opto-couplers form the driver circuit for MOSFET. The output from driver circuits is given across the gate and source of the MOSFET. Then the individual bridge output are shown below.

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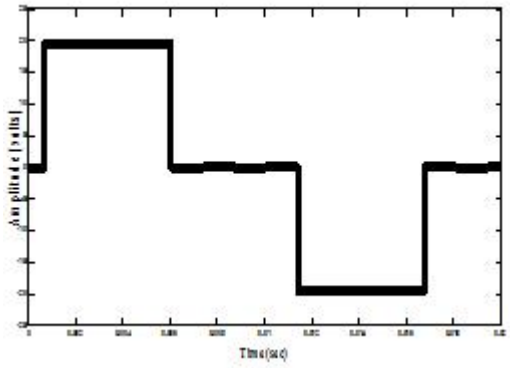

Fig.6 Output of bridge H_2

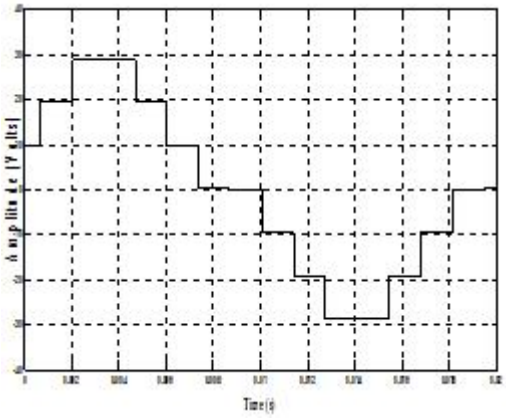

Fig.7 Seven-level output of asymmetric cascaded MLI using Digital Modulation

TABLE II. COMPARISON OF PERFORMANCE PARAMETERS

Performance Parameters	Digital Modulation	Conventional Modulation
THD (Voltage)	9.79%	15.06%
DF_1	2.57%	0.1%
DF_2	1.15%	2%
Switching losses	3.9850W	3.9850W

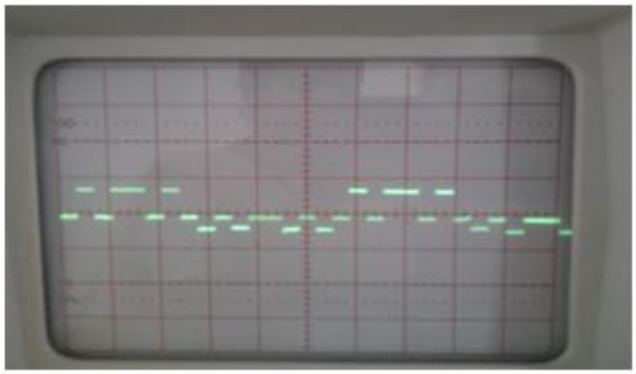

Fig.8 Output of Bridge-1for digital modulation technique

VI. CONCLUSION

This paper provides a clear overview on a new modulation technique employed in generating the pulses required to trigger the semiconductor devices used in multilevel inverters. This proposed model helps to optimize the number of levels using two sources with fundamental frequency switching. So the efficiency of the system is also improved. Further by increasing the number of stages, the THD can be reduced to a low value and the output voltage and is almost same as the sinusoidal voltage. This proposed system eliminates the complexity of generating gate signals when the stages are added. The performance parameters such as THD, DF_1, DF_2 and switching losses has been calculated for both digital modulation and hybrid modulation techniques. From the analysis and comparisons made, it was found that the digital modulation technique has reduced THD. The switching losses of the devices used in the circuit are calculated for various switching frequencies. This paper also employs asymmetrical DC sources which reduces the number of bridges used thus decreasing the complexity and cost of the circuit.

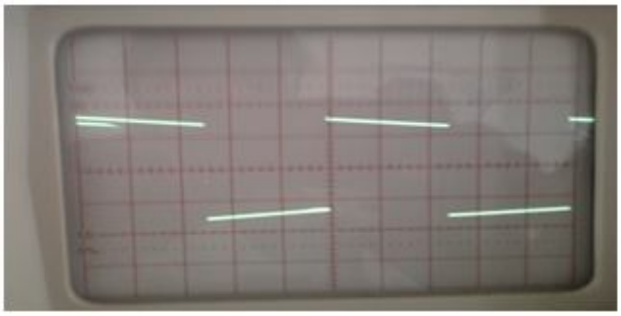

Fig.9 Output of Bridge-2 for digital modulation technique

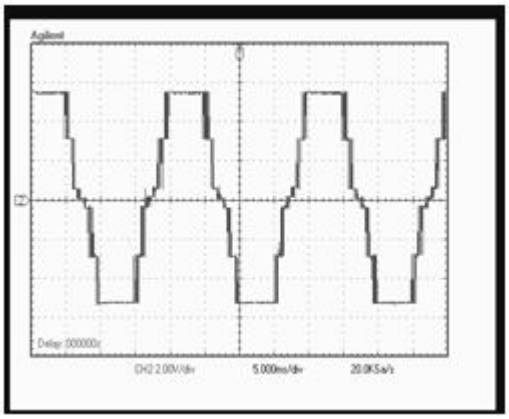

Fig.10 Load voltage waveform for MLI using digital modulation

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